ABSTRACT OF THE DISCLOSURE

Disclosed herewith is a semiconductor data processing device that realizes low power consumption at the standby time and at the operation time, as well as speeds up the interfacing operation. The semiconductor data processing device can connect a non-volatile storage device to a general-purpose bus of a host system. The data processing device enters the active or standby state in response to the state of the general-purpose bus. In the standby state, the data processing device stops the internal clock signal and applies a substrate bias voltage to each object so as to suppress the potential sub-threshold leak current therefrom. This bias voltage is also applied to the central processing unit and the rewritable non-volatile memory for storing a control program to be executed by the central processing unit. The central processing unit processes data in units of n bits or below when the interface controller and the data transfer controller input/output parallel data in units of 2n bits.